Listing of the Claims

This listing of the claims will replace all prior versions and listings of the claims in the application:

1. (original) A method of reboot reporting comprising:

reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors;

generating at least one non-maskable interrupt signal;

outputting the non-maskable interrupt signal to a processor of the plurality of computer systems;

outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems; and

generating an indication that at least one computer system has a fault condition.

2. (original) The method of claim 1 further comprising associating the non-maskable interrupt signal with at least one computer system of the plurality of computer systems.

3. (original) The method of claim 2 further comprising generating a notice identifying the at least one computer system.

4. (original) The method of claim 3 further comprising redistributing the processing load from the at least one computer system to the remaining plurality of computer systems.

5. (original) The method of claim 1 further comprising counting the number of times the non-maskable interrupt signal is generated.

6. (original) A system for reboot reporting comprising:

a plurality of computer systems having at least one processor and at least one non-maskable interrupt output;

a manager system in circuit communication with the plurality of computer systems and comprising at least one non-maskable interrupt input associated with the plurality of computer systems.

7. (original) The system of claim 6 wherein the plurality of computer systems comprises a plurality of non-maskable interrupt outputs and the manager system comprises a plurality of non-maskable interrupt inputs.

8. (original) The system of claim 7 wherein the non-maskable interrupt outputs of the plurality of computer systems are in circuit communication with the plurality of non-maskable inputs of the manager system.

9. (original) The system of claim 6 wherein the plurality of computer systems comprises at least one computer system having a processor, a first bridge circuit and a second bridge circuit and wherein the second bridge circuit comprising a non-maskable interrupt signal output in circuit communication with the processor.

10. (original) The system of claim 9 wherein the non-maskable interrupt output of the second bridge is in circuit communication with the manager system.

11. (original) The system of claim 6 further comprising logic for reading at least one non-maskable interrupt input associated with the plurality of computer systems.

12. (original) The system of claim 11 further comprising logic for generating an indication that at least one computer system has a fault condition based on the presence of a non-maskable interrupt signal present on the at least one non-maskable interrupt input.

13. (currently amended) A system for reboot reporting comprising:
a plurality of computers **comprising at least one means for processing**;
means for managing the plurality of computers; and

means for outputting a non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers to the means for managing **and to the at least one means for processing**.

14. (original) The system of claim 13 further comprising means for detecting the non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers and generating a detection signal in response thereto.

15. (original) The system of claim 13 further comprising means for generating at least one non-maskable interrupt signal.

16. (original) The system of claim 13 further comprising means for generating an indication that at least one computer has a fault condition.

17. (original) The system of claim 13 further comprising means for associating the non-maskable interrupt signal with at least one computer of the plurality of computers.

18. (original) The system of claim 17 further comprising means for redistributing the processing load from the at least one computer to the remaining plurality of computers.

19. (original) The method of claim 13 further comprising means for counting the number of times the non-maskable interrupt signal is generated.

20. (original) A computer system comprising:

a processor;

a memory;

at least one bridge circuit in circuit communication with the processor;

a non-maskable interrupt signal circuit in circuit communication with the processor and at least one other computer system.

21. (original) The system of claim 21 wherein the at least one other computer system comprises an enclosure manager.

22. (original) A system comprising:

an enclosure having a plurality of individual computer systems and a manager computer system;

wherein at least one of the plurality of computer systems comprises a processor and a non-maskable interrupt signal circuit, the non-maskable interrupt signal circuit in communication with the processor and the manager computer system, the non-maskable interrupt signal circuit comprising a bridge circuit and a non-maskable interrupt signal path to the processor and the manager computer system.

23. (original) The system of claim 22 wherein the manager computer system comprises a non-maskable interrupt signal input.

24. (original) The system of claim 23 wherein the manager computer system comprises logic for reading a state of the non-maskable interrupt signal input.

25. (original) The system of claim 24 wherein the manager computer system comprises logic for generating a notice based on the state of the of the read non-maskable interrupt signal input.

26. (original) A system comprising:

means for housing a plurality of digital devices;

means for managing the plurality of digital devices, said means for managing comprising a location within said means for housing;

means for receiving and processing executable instructions, said means for receiving and processing comprising a location within said means for housing;

means for generating a non-maskable interrupt signal; and

means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means for managing.

27. (original) The system of claim 26 wherein the means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means for managing comprising a non-maskable interrupt signal pathway.

28. (original) The system of claim 26 wherein the means for managing the plurality of digital devices comprises means for reading the state of the means for communicating and means for generating a notice based on the state of the means for communicating.

29. (original) The system of claim 26 wherein the means for managing the plurality of digital devices comprises means for re-distributing a processing distribution among the plurality of digital devices.

30. (original) The system of claim 26 wherein the means for generating a non-maskable interrupt signal comprises a bridge circuit associated with the means for receiving and processing.